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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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Title of Invention	DUAL SCAN CHAIN DESIGN METHOD AND APPARATUS

Application Number : 10/718445

Confirmation Number: 9844

First Named Applicant: Sandeep Bhatia

Attorney Docket Number: CA7035962001

Art Unit: 2138

Examiner: John J Tabone Jr

Search string: (6377912 or 6694464 or 6574762 or 6114892 or 6158032 or 20050015689).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
JJT	1	6377912	2002-04-23	Sample et al.	B1		
	2	6694464	2004-02-17	Quayle et al.	B1		
	3	6574762	2003-06-03	Karimi et al.	B1		
	4	6114892	2000-09-05	Jin			
	5	6158032	2000-12-05	Currier et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
JJT	1	20050015689	2005-01-20	Eppensteiner et al.	A1		

Signature

Examiner Name	Date
/John J. Tabone Jr/ (10/10/2006)	

PTO/SB/08B(07-05)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/718,445
Filing Date	November 19, 2003
First Named Inventor	Sandeep Bhatia
Art Unit	2138
Examiner Name	John J. Tabone, Jr.
Attorney Docket Number	CA7035962001

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
JJT	1	BALAKRISHNAN, K. J., et al., *"Deterministic Test Vector Decompression in Software Using Linear Operations"*, Proceedings of the 21st IEEE VLSI Test Symposium, April 27 - May 1, 2003, pp. 225 - 231, IEEE, Los Alamitos, CA, USA.	
	2	BARDELL, P. H. et al., *"Build-In Test for VLSI: Pseudorandom Techniques"*, 1987, pp. 61-313, John Wiley and Sons, New York, USA.	
	3	BHATIA, S., *"Test Compaction by Using Linear-Matrix Driven Scan Chains"*, Proceedings of the 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, November 3 - 5, 2003, pp. 185 - 190, IEEE, USA.	
	4	BHATIA, S., *"Test Compaction in a Parallel Access Scan Environment"*, Proceedings of the 6th Asian Test Symposium (ATS '97), November 17 - 19, 1997, pp. 300 -305, IEEE, Los Alamitos, CA, USA.	
	5	HELLEBRAND. S., et al., *"Generation of Vector Patterns Through Reseeding of Multiple-Polynomial Linear Feedback Shift Registers"*, Proceedings of the International Test Conference, 1992, pp. 120 -124, France.	
	6	HSU, F. F. et al., *"A Case Study on the Implementation of the Illinois Scan Architecture"*, Proceedings of the International Test Conference; 2001, pp. 538 - 547, International Test Conference, Washington, D.C., USA.	
	7	KIEFER, G. et al., *"Deterministic BIST with Multiple Scan Chains"*, Proceedings of the International Test Conference, 1998, pp. 1057 - 1064, International Test Conference, Washington, D.C., USA.	
	8	KRISHNA, C.V. et al., *"Reducing Test Data Volume Using LFSR Reseeding with Seed Compression"*, Proceedings of the International Test Conference, 2002, pp. 321 - 330, International Test Conference, Washington, D.C., USA.	
	9	McCLUSKEY, E. J., *"Test Data Compression"*, Design & Test of Computers, March - April 2003, pp. 76 - 87, Volume 20, Issue 2, IEEE Computer Society and the IEEE Circuits and Systems Society, USA.	
↓	10	RAJSKI, J. et al., *"Embedded Deterministic Test for Low Cost Manufacturing Test"*, Proceedings of the International Test Conference, 2002, pp. 310 - 310, International Test Conference, Washington, D. C., USA.	

Examiner Signature	/John J. Tabone Jr/ (10/10/2006)	Date Considered	

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